

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AMENDMENT "A"

APPLICANT(S): Tohisharu Yanagida OLD DOCKET NO.: P99,1318  
NEW DOCKET NO.: 09792909-4298  
SERIAL NO.: 09/385,959 GROUP ART UNIT: 2814  
DATE FILED: August 30, 1999 EXAMINER: D. Graybill  
INVENTION: "SEMICONDUCTOR APPARATUS AND PROCESS OF  
PRODUCTION THEREOF"

Hon. Assistant Commissioner for Patents  
Washington, DC 20231

S I R:

This Amendment "B" is filed in response to the Office Action of September 4, 2001.  
Please reconsider the application in view of the amendment and remarks presented below.

IN THE DRAWINGS

Please amend FIGs. 11, 12A, 12B, 12C, 13A, and 13B as shown on the drawing  
copies marked in red and attached to the Request for Approval of Drawing Changes  
submitted herewith.

IN THE CLAIMS

Please amend claims 9, 10, and 20 as follows:

9. (Amended) A process of production of a semiconductor apparatus as set forth in claim  
7, in said third step, the surfaces of the bumps are chemically activated in parallel to the cleaning  
of the surfaces of the bumps.

10. (Amended) A process of production of the semiconductor apparatus as set forth in  
claim 7, wherein, in said third step, any resin film components deposited on said bumps are  
removed.

20. (Amended) A process of production of a semiconductor apparatus as set forth in  
claim 19, wherein said solder bumps have a melting point higher than a melting point of said  
solder layers and said solder layers are comprised of a eutectic solder.

### REMARKS

Claims 1-24 are pending in the application. Claims 1-6 are withdrawn from consideration as being directed to non-elected inventions. In the Office Action of September 4, 2001, the Examiner made the following disposition:

- A.) Objected to the drawings.
- B.) Rejected claims 9, 10, 20, and 21 under 35 U.S.C. §112, second paragraph.
- C.) Rejected claims 7-11, 16, and 19-24 under 35 U.S.C. §102(e) as being anticipated by *Hayes*.
- D.) Rejected claims 12, 13, and 17 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Nishikawa et al.* and *Denning et al.*
- E.) Rejected claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Nishikawa et al.* and *Denning et al.* and further in view of *Okumura*.
- F.) Rejected claim 18 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Jackson*.

Applicant respectfully traverses the rejections. Applicant addresses the Examiner's disposition as follows:

A.) Objection to the drawings:

Figures 11, 12A, 12B, 12C, 13A, and 13B have been amended as per the Examiner's request to overcome the objection.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

B.) Rejection of claims 9, 10, and 20 under 35 U.S.C. §112, second paragraph:

Claims 9, 10, and 20 have been amended as per the Examiner's request to overcome the rejection. Claim 21 depends indirectly or directly from claim 20 and is therefore allowable for at least the same reasons that claim 20 is allowable.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

C.) Rejection of claims 7-11, 16, and 19-24 under 35 U.S.C. §102(e) as being anticipated by *Hayes*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 claims a process of production of a semiconductor apparatus, wherein in a first step, metal bumps are formed to connect to a circuit pattern of a semiconductor device. In a second step, a resin film is formed on the surface of the semiconductor device to seal spaces between the bumps and to become thinner than a height of the metal bumps. In a third step, the surfaces of the metal bumps projecting out from the resin film are cleaned.

This is clearly unlike *Hayes*, which fails to disclose Applicant's first, second, and third claimed steps. Referring to *Hayes* Figs 2 and 3, *Hayes* discloses forming solder columns 3, instead of bumps, to connect to a circuit pattern 2 of a semiconductor device 5. A polymer film 4 is then deposited between the solder columns 3. A top surface of the polymer film 4 is then removed to expose tops of the solder columns 3. Then, solder bumps 9 are formed onto the tops of the solder columns 3. The *Hayes* solder bumps 9 are neither formed to connect to the circuit pattern 2 (unlike Applicant's claimed step 1), nor sealed by resin film 4 (unlike Applicant's claimed step 2), nor cleaned (unlike Applicant's claimed step 3).

The Examiner has interpreted *Hayes* solder columns 3 to anticipate Applicant's solder bumps, however, *Hayes* solder columns 3 fail to disclose or even suggest Applicant's solder bumps. *Hayes* solder columns 3 are merely provided as bases for *Hayes*'s solder bumps 9. Unlike Applicant's claimed solder bumps, *Hayes*'s solder columns 3 are not provided for flip-chip-type connection, while its solder bumps 9 are so provided. *Hayes*'s solder columns 3 are merely provided for supporting solder bumps and, thus, fail to anticipate Applicant's solder bumps. Accordingly, for at least this reason, *Hayes* cannot anticipate Applicant's claim 7.

Further, unlike Applicant's claimed solder bumps, *Hayes*'s solder bumps 9 are neither sealed by resin nor cleaned. This clearly teaches away from Applicant's claimed invention, wherein Applicant's solder bumps are sealed with resin to provide strength and cleaned for greater adhesion. Instead, *Hayes*'s solder bumps 9 are fully exposed and thus subject to breakage. In fact, *Hayes* fails to even discuss that its solder bumps 9 are cleaned.

Claims 8-11, 16, and 19-24 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

D.) Rejection of claims 12, 13, and 17 under 35 U.S.C. §103(a) as being unpatentable over Hayes in view of Nishikawa et al. and Denning et al.:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is not anticipated by *Hayes* as discussed above. Further, since *Hayes* fails to disclose or even suggest Applicant's claimed steps, *Hayes* fails to disclose or suggest Applicant's claim 7.

*Nishikawa et al.* and *Denning et al.*, taken singly or in combination, still fail to disclose or suggest solder bumps that are formed to connect to the circuit pattern, or sealed by resin film, or cleaned. Thus, *Hayes* in view of *Nishikawa et al.* and *Denning et al.* still fails to disclose or suggest Applicant's independent claim 7.

Claims 12, 13, and 17 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

E.) Rejection of claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over Hayes in view of Nishikawa et al. and Denning et al. and further in view of Okumura:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes* in view of *Nishikawa et al.* and *Denning et al.* as discussed above.

*Okumura* still fail to disclose or suggest solder bumps that are formed to connect to the circuit pattern, or sealed by resin film, or cleaned. Thus, *Hayes* in view of *Nishikawa et al.* and *Denning et al.* and further in view of *Okumura* still fails to disclose or suggest Applicant's independent claim 7.

Claims 14 and 15 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

F.) Rejection of claim 18 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Jackson*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes* as discussed above.

*Jackson* still fail to disclose or suggest solder bumps that are formed to connect to the circuit pattern, or sealed by resin film , or cleaned. Thus, *Hayes* in view of *Jackson* still fails to disclose or suggest Applicant's independent claim 7.

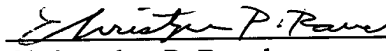
Claim 18 depends directly or indirectly from claim 7 and is therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

#### CONCLUSION

In view of the foregoing, it is submitted that claims 1-24 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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